Silicon field-effect transistor based on quantum tunneling

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This letter explores regulation of current flow within a silicon field-effect transistor by gate-induced tunneling through a Schottky barrier located at the interface between a metallic source electrode and the Si channel. The goal here is to forestall short-channel effects which are expected to prevent further size reductions in conventional devices when linewidths reach ~1000 Å. Control of tunneling appears to be possible at minimum channel lengths $L \sim 250$ Å or less while simultaneously eliminating the need for large-area source and drain contacts, so that scaling of Si transistors could be significantly extended if this principle proves technically feasible.

Extraordinary progress has resulted from a doubling in the number of individual transistors within the most advanced integrated circuits every two or three years over the past three decades. Conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) are thought to be limited to minimum dimensions $\gtrsim$1000 Å, however, so that further increases in device density are expected to slow within the next ten years as production linewidths approach this scale.[1] Channel lengths as small as $L \approx 300$ Å appear theoretically possible by employing a bottom gate as well as a top gate,[2] but this highly modified structure presents formidable challenges to future fabrication technology. Recently, n-MOSFETs with gate lengths $L \approx 400$ Å have been fabricated[3] utilizing a sophisticated phosphorus diffusion technique to produce ultrathin source and drain fingers with junction depths $t \approx 100$ Å. Here we propose a different alteration in the standard MOSFET structure which could extend scaling limits into the range $L \sim 250$ Å, based upon control of quantum tunneling through a Schottky barrier formed at the interface between a metallic source electrode[4] and the Si channel.

The simplest (idealized) structure of this type is sketched in Fig. 1. The essential departure from a standard MOSFET is the use of metal or silicide at the source and drain electrodes in order to present a Schottky barrier of constant height, Φ_B, to carriers entering the Si channel. Fabrication difficulties include the need for uniform barrier heights and an accurately planar surface extending from source to channel to drain following deposition of the metallic electrodes. The gate is to be separated from the Si channel by a very thin dielectric, ε_i, of thickness $d < 50$ Å. Illustrated here in self-aligned configuration, the gate could be offset in order to permit a shallow implant of the finished device to convert the drain to a low-impedance ohmic contact. The Si substrate is undoped for simplicity in the example described below, so that the channel region beneath the gate will be depleted of carriers under flat-band conditions. The flat-band voltage in this case is just the difference in work functions between gate and source electrodes. With positive applied gate voltage V_G (relative to flat-band), large electric fields are induced at the interface between the grounded source and the Si channel, $\varepsilon_s = 11.8\ \varepsilon_0$, close to the surface. This region of high electric fields and rapid band-bending extends only to distances of order $\tilde{d} = (\varepsilon_s/\varepsilon_i)d$ near the top corner of the reverse-biased source electrode in both the longitudinal, x, and vertical, z, directions. The potential is pinned near V_D at the forward-biased drain contact, and electrons will populate a surface channel beneath the gate when $V_G > \Phi_B + V_D$.

We have simulated the structure shown in Fig. 1 using a commercial package, SEMICAD,[5] together with our own calculation of tunneling and thermionic emission at the source contact in order to achieve a self-consistent solution. Results are reported here for Schottky barrier heights $\Phi_B = 0.37$ eV at the source and drain. This value is large enough that thermionic emission currents ~10 A/cm^2 are small at room temperature. No common material produces an n-type barrier less than 0.55 eV on Si, but lower p-type barriers are readily available. Pd_2Si has a barrier $\Phi_B = 0.37$ eV to p-type Si, while Au contacts yield $\Phi_B = 0.32$ eV. Several additional silicides have p-type barriers $\Phi_B \approx 0.40$ eV, so that the example chosen here represents many possible choices for metallization. In the p-channel version of the device, a negative gate voltage controls the tunneling of light holes, with effective mass $m^*_{lh} = 0.16 m_0$, out of the source electrode and into the surface channel. The insulator here is SiO_2 ($\varepsilon_i = 3.9\varepsilon_0$) with thickness $d = 30$ Å, the minimum oxide thickness currently employed in experimental devices and close to the limit set by tunneling.[6] Depth of source and drain electrodes and gate thickness is $t = 100$ Å, although these dimensions are not

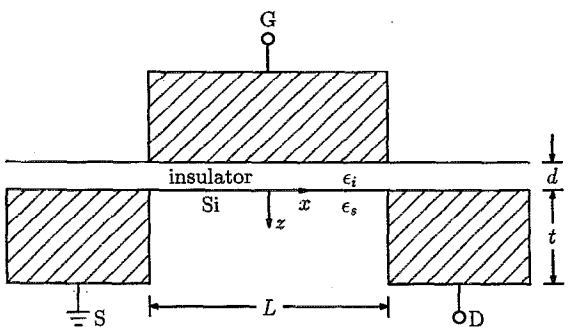

FIG. 1. Sketch of tunneling MOSFET structure with Schottky barrier contacts at metallic source and drain electrodes coplanar with the Si channel. Tunneling of carriers is controlled via gate-induced electric fields at the interface between the grounded source S and the Si channel of length L.

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critical. The maximum gate voltage in these simulations is 2.0 V corresponding to an insulator electric field $F_i=6.7\times10^6$ V/cm, a factor of 3–4 below breakdown for such ultrathin SiO_2 layers[7] and roughly equal to the largest field consistent with a ten-year lifetime.[6] Reverse tunneling can occur at the drain for large V_D with the gate grounded, as a few electrons penetrate the larger complementary barrier $\Phi_B^n=0.75$ eV. This effect would produce a significant subthreshold current $\sim10^{-3}$ A/cm, but is neglected here because it can be easily eliminated by gate offset and/or ion implantation.

The tunnel current density at the source can be estimated by adapting an approximate expression derived by Padovani and Stratton[8] for reverse-biased Schottky barriers:

$$j\approx\frac{K}{c_F^2}\exp(-b_F)[1-\exp(-c_F V_D)] \tag{1}$$

with effective Richardson constant $K=1.6\times10^{10}(m^*/m_0)$ A cm^{-2} eV^{-2}. In the triangular barrier approximation, the WKB penetration probability b_F for carriers at the source Fermi energy is given in terms of electric field by the Fowler–Nordheim expression for internal field emission:

$$b_F=0.683(m^*/m_0)^{1/2}\frac{\Phi_B^{3/2}\ (\text{eV})}{F_s(\text{V/Å})}, \tag{2}$$

with energy derivative $c_F=3b_F/2\Phi_B$. These expressions indicate that semiconductor electric fields $F_S\sim2\times10^6$ V/cm are required to induce large tunnel current densities $j\sim10^6$ A/cm with $\Phi_B=0.37$ eV and $m^*=0.16\ m_0$. Fields of this magnitude are indeed generated within distances $\sim\tilde{d}/3$ near the top corner of the source electrode under the conditions described above. In the detailed simulations, we evaluate transmission probabilities numerically by solving the Schrödinger equation and summing over energy,[9] taking into account spatial variations of electric field within the barrier, barrier lowering due to the classical image potential, and thermionic emission.[10] Although drift and diffusion within the conducting surface layer are included, the associated channel resistance is negligible for $L<1000$ Å.

Figure 2(a) shows a contour plot of the tunnel barrier near the source electrode as a function of depth z below the Si surface and distance x along the channel, computed for $V_G=2.0$ V and $V_D=1.0$ V with $L=500$ Å. Each line represents an increment of 0.05 eV in potential energy, the uppermost solid curve marking the exit point for carriers tunneling at the source Fermi energy. The predicted current density in Fig. 2(b) peaks to $j\sim10^6$–10^7 A/cm within the first ~20 Å below the surface, and then decays more slowly with distance. We note that the thickness and current density of this near-surface region are roughly similar to the channel region of a conventional MOSFET in the hard "on" condition, although the carrier concentration inside the tunnel barrier is of course much smaller.

Figure 3 illustrates calculated output characteristics for two different channel lengths, $L=500$ and 250 Å, showing drain current I_D in A/cm of channel width (perpendicular to the plane of Fig. 1) versus drain voltage V_D at several values of gate voltage V_G. The behavior shown in the solid curves

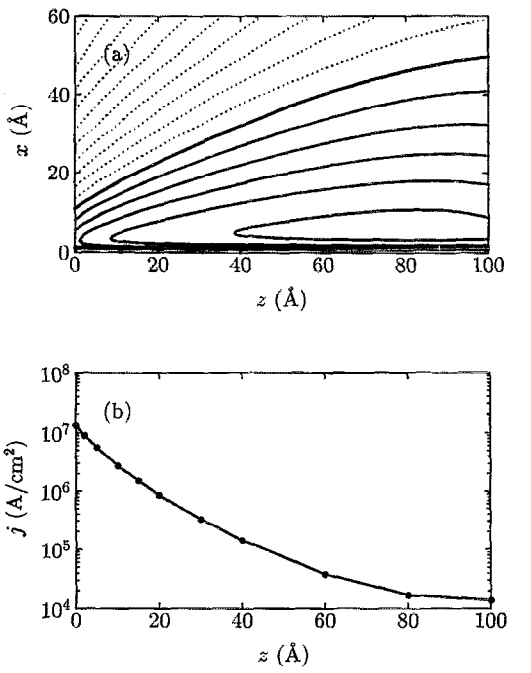

FIG. 2. (a) Contour plot of tunnel barrier and electrostatic potential within the Si channel near its interface with source electrode, computed for $V_G=2.0$ V, $V_D=1.0$ V, and $L=500$ Å as a function of distance, x along the channel and depth z below the Si surface. Each line represents an increment of potential energy in intervals of 0.05 eV, the uppermost solid curve marking the exit point for carriers tunneling at the source Fermi energy through a Schottky barrier $\Phi_B=0.37$ eV. (b) Calculated tunnel current density vs depth in this example.

of Fig. 3(a) for $L=500$ Å appears similar to a conventional MOSFET with threshold voltage $V_T\approx1.0$ V, although the underlying physics is entirely different. Short-channel effects, barely noticeable here, are absent at longer gate lengths. The relatively slow saturation with drain voltage is due to partial screening of the source electric field by carriers populating the surface conducting layer. As V_D is increased, these surface charges are drawn away from the source, allowing gate-induced electric fields to approach their limiting values set by the "bare" potential. The leakage current $\sim10^{-5}$ A/cm with $V_G=0$ in Fig. 3(b) represents thermionic emission over the source Schottky barrier, and could be greatly reduced by moderate doping of the channel region. The dotted characteristics shown in Fig. 3 for $L=250$ Å are also similar to those of a conventional MOSFET, but one which now shows pronounced short-channel effects near its minimum useable channel length within this configuration. When switched at $V_G=2.0$ V, the product of channel resistance and gate capacitance yields time constants of ~3.5 and 8 ps for $L=250$ and 500 Å, respectively.

The effect of finite channel length may be qualitatively understood in terms of the characteristic size, $\tilde{d}=(\varepsilon_s/\varepsilon_i)d$, of the regions of high electric field concentrated near the source and drain. For SiO_2 insulator thickness $d=30$ Å, this scale is $\tilde{d}\approx90$ Å. Gate lengths $L>4\tilde{d}$ approach the long-channel limit, while for $L<3\tilde{d}$ the source and drain are no longer effectively isolated and control via the gate becomes lost. Device characteristics depend upon the ratio d/L for a

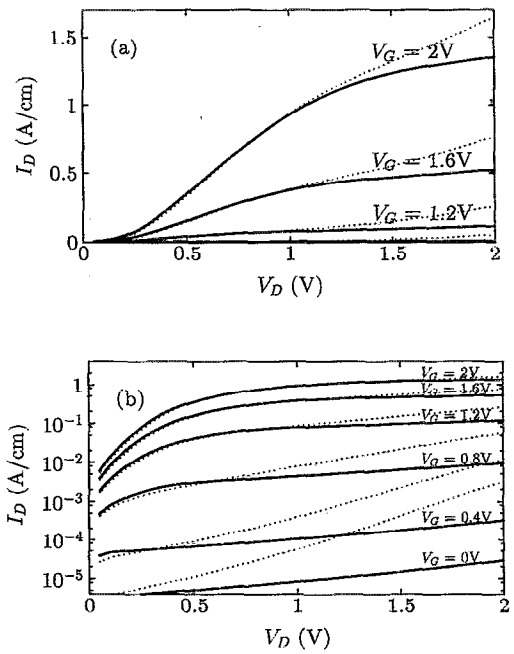

FIG. 3. Calculated output characteristics showing drain current I_D vs drain voltage V_D, as a function of gate voltage V_G relative to flat-band. Schottky barrier height is Φ_B=0.37 eV, carrier effective mass is m^*=0.16m_0, gate insulator is SiO_2 with thickness d=30 Å, and results are shown for channel lengths L=500 Å (solid lines) and 250 Å (dotted curves) in (a) linear and (b) log format.

given dielectric, and will thus remain approximately constant if all distances and voltages are scaled by the same factor. With d=40 Å, for example, the gate lengths in Fig. 3 would be L=667 and 333 Å and the maximum voltage 2.67 V. Use of Si_3N_4(ε_i=7.5ε_0) as the gate insulator could potentially reduce the distance and voltage scales by a factor of ~2, implying minimum gate lengths ~150 Å and supply voltages ~1 V.

In summary, we have demonstrated that gate-induced band-bending within a Si MOSFET structure can be sufficient to induce internal field emission through a Schottky barrier formed at a metal or silicide source electrode. Because the height of this barrier remains approximately constant, short-channel effects can be forestalled to gate lengths as small as L~250 Å while retaining SiO_2 as the gate insulator. Conventional source and drain contacts are no longer required, since these can be integrated into the lowest-level wiring pattern and placed in the substrate. This reduces total device length, eliminates contact resistances, and provides enhanced flexibility in the design of interconnects, all of which pose serious problems for conventional MOSFETs at these dimensions. Although exceptionally tight control of the *vertical* fabrication technology is required, no critical dimensions are lithographically defined. Control of Schottky barrier tunneling via a field effect represents, we believe, a new principle for nanoscale electronics that deserves to be explored. Many alternative configurations are possible, including opportunities for complementary devices and CMOS-type architectures.

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